## MICROMACHINE™ SERIES

#### MICROMACHINE™

MicroMachine\* devices are complete 8-bit microcomputers on single MOS integrated circuits. The family can execute the F8 instruction set of more than 70 commands, allowing expansion into multi-chip configurations with software compatibility. The devices feature read only memory, 64 bytes of scratchpad RAM, a programmable binary timer, 32 bits of I/O, and a single +5 V power supply requirement.

Members of the family differ in memory type and size. The F3870 has 2048 bytes of mask programmed ROM while the F38E70 has 2048 bytes of PROM. The F3872 has 3K bytes of masked ROM plus 64 bytes of RAM. The additional RAM is addressed from the program and data counters, not the ISAR. The F3874 contains 4096 bytes of masked programmed ROM.

Utilizing ion-implanted, n-channel silicon-gate technology and advanced circuit design techniques, Fairchild's single-chip microcomputers offer maximum cost effectiveness in a wide range of control and logic replacement applications.

### STROBE 8-BIT I/O PORT 8-BIT I/O PORT +5 V ALU 64 x 8 GND -RAM ACCUMULATOR PROGRAM COUNTER ISAR TEST -TEST SEQUENCER STACK REGISTER RESET **POWER-ON RESET** DATA COUNTER XTL 1 CLOCK LOGIC DATA COUNTER 2 TIMER See Fig. 3 2048 x 8 ROM INTERRUPT 8-BIT I/O PORT 8-BIT I/O PORT

### **DEVELOPMENT SUPPORT**

The Formulator family of development equipment supports the F3870, the one-chip micromachine manufactured by Fairchild. The Formulator Operating System, Utility Programs, and the Fairbug Monitor are totally compatible with the F3870, since it shares the same instruction set with the Formulator. A Simulation (Quad I/O) Module and an In-Circuit Emulation (ICE) cable are available to extend the Formulator features to the user's prototype or production breadboard. This creates a powerful design tool for creating the user's own F3870 software. In addition, the F3870 Emulator, a single stand-alone module for emulating the final F3870 software in PROMs, is available for building prototype systems.

#### **F3870 SIMULATION**

The non-microprocessor elements of the user's hardware configuration can be assembled on a breadboard and connected to Mark I, II, IIFD, III or IIIFD via the ICE cable plugged into a 40-pin socket on the user's board. The cable connector on the Processor Module in the Formulator provides I/O ports 0 and 1, while the Simulation (Quad I/O) Module provides I/O ports 4 and 5. This system provides real-world simulation of the user's components in their actual environment with the vital microprocessor signals, including the complete software debugging features of the Formulator, cabled to the external breadboard.

#### **F3870 EMULATOR**

After F3870 ROM codes are frozen, a smaller, easier-to-handle and less expensive tool is required. To accomplish this design-in task, Fairchild has developed the F3870 Emulator. The F3870 Emulator contains sockets for two 2708s or two 2716 EROMs in place of the F3870 on-chip ROM so ROM codes can be verified and easily changed. The F3870 Emulator plugs directly into the F3870 40-pin socket in the production prototype using a short Emulator cable. The printed circuit module is approximately 5" by 7".

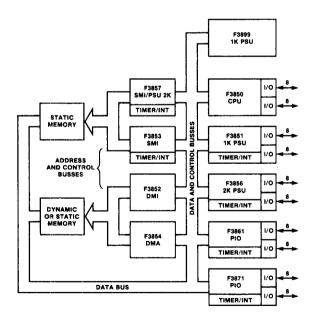
## MICROCOMPUTER TRAINING COURSES

Fairchild offers training courses which are aimed at the design engineer who must learn to design the microprocessor into a working system. Both software (instruction sets) and hardware related instruction is given. Emphasis is placed on "hands-on" instruction with microprocessor development systems.

To achieve this understanding, the courses cover the details of I/O ports, use of subroutines and interrupts, where and how the ROM and RAMs are attached to the CPU and how to interface with static or dynamic memories.

Two separate four day courses are offered. One covers the F8 device family and the Micromachine series hardware and software design. The other course covers the F6800 device family in the same manner. An optional fifth day allows instruction in the alternate microprocessor.

## **F8 MICROPROCESSOR FAMILY**



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## **F8 MICROPROCESSOR FAMILY**

## **FEATURES**

FUNCTION	F3850 CPU	F3851 PSU	F3852 DMI	F3853 SMI	F3854 DMA	F3856 PSU	F3857 PSU/SMI	F3861 PIO	F3871 PIO	F3899 ROM
Arithmetic Unit Accumulator 64-byte Scratchpad RAM	Yes Yes Yes									
Power on Detect Clock Circuits Interrupt Logic	Yes Yes Yes	Yes		Yes		Yes	Yes	Yes	Yes	
Instruction Register I/O Ports (8 lines each) ROM (K bytes)	Yes 2	2 1K				2 2K	2K	2	2	1K
Data Bus (8 lines) Address Bus (16 lines) Control Bus (5 lines)	Yes Yes	Yes Yes	Yes Yes Yes	Yes Yes Yes	Yes Yes Yes	Yes Yes	Yes Yes Yes	Yes Yes	Yes Yes	Yes Yes
Program Counter Stack Register Data Counters		Yes Yes 1	Yes Yes 2	Yes Yes 2		Yes Yes 2	Yes Yes 2			Yes Yes 1
Programmable Timer External Interrupt Pulse Width Measure		Yes Yes		Yes Yes		Yes Yes Yes	Yes Yes Yes	Yes Yes	Yes Yes Yes	
Event Counter Vectured Interrupts Memory Refresh Control DMA Control		Yes	Yes Yes	Yes	Yes	Yes Yes	Yes Yes	Yes	Yes Yes	
+5V required +12V required Power mW (Typ)	Yes Yes 330	Yes Yes 270	Yes Yes 330	Yes Yes 330	Yes Yes 280	Yes Yes 785	Yes Yes 785	Yes Yes 270	Yes Yes 270	Yes Yes 270
Maximum # in System	1	63	1	1	4	31	1	62	62	63
Logic/Connection Diagram	P1	P2	P3	P4	P5	P6	P7	P2	P6	P8
Package(s)	61,8P	61,8P	61,8P	6I,8P	61,8P	61,8P	61,8P	61,8P	61,8P	61,8F

Number of ports in System is limited by addressing. The maximum is 256 Port Adresses (each F8 device uses 4 Port Addresses). Maximum memory is 64K bytes RAM/ROM/PROM.

The F38T56 and F38T57 incorporate the F3871-type of timer logic and strobe logic. These devices will be available 3rd quarter 1978.

## **PORT ADDRESSING**

## **F8 MICROPROCESSOR FAMILY**

	DEVICE NO.	PORT A		PORT B		PORT C		PORT D		TIMER INTERRUPT	
Item		ADDR.	FUNC.	ADDR.	FUNC.	ADDR.	FUNC.	ADDR.	FUNC.	VECTOR ADDRESS	PORT TYPES
1	F3850	0	I/O	1	1/0						Standard
2	F3851	XXXXXX00	1/0	XXXXXX01	1/0	XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
3	F3851A	4	1/0	5	I/O	6	Control	7	Timer	H'0020'	Standard
4	F3852	H,OC,		H'OD'	Control	H'OE'		H'OF'			
5	F3852/ SL31116	H'EC'		H'ED'	Control	H'EE'		H'EF'			
6	F3853	H'OC'	Interrupt Vector Addr. Lo	HʻOĐ'	Interrupt Vector Addr.Hi	H'OE'	Control	H'OF'	Timer	Software Programmable	
7	F3854	1111YY00	DMA Mem. Addr. Lo	1111YY01	DMA Mem. Addr. Hi	1111YY10	Control Hi Count	1111YY11	Lo Count		
8	F3856	XXXXXX00	1/0	XXXXXY01	1/0	XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
9	F38T56	XXXXXX00	1/0	XXXXXY01	I/O	XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
10	F3856A	8	I/O	9	I/O	H'OA'	Control	Н'ОВ'	Timer	H'0024'	Standard
11	F3857					XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
12	F3861A	4	1/0	5	I/O	6	Control	7	Timer	H'0600'	Standard
13	F3861B	8	1/0	9	I/O	H'A'	Control	H'B'	Timer	H'0340'	Standard
14	F3861C	H'20'	1/0	H'21'	I/O	H'22'	Control	H'23'	Timer	H'0320'	Standard
15	F3861D	H'24'	1/0	H'25'	I/O	H'26'	Control	H'27'	Timer	H'0360'	Standard
16	F3861E	4	1/0	5	I/O	6	Control	7	Timer	H'0020'	Standard
17	F3871E	4	1/0	5	I/O	6	Control	7	Timer	H'0020'	Standard
18	F3871F	4	1/0	5	I/O	6	Control	7	Timer	H'0020'	Direct Drive
19	F3871G	4	1/0	5	I/O	6	Control	7	Timer	H'0020'	Open Drain
20	F3871H	4	1/0	5	I/O	6	Control	7	Timer	H'0420'	Standard

<sup>1.</sup> XXXXXX is a Mask Option

<sup>2.</sup> YY is a Pin Strap Option (1111YY00)

<sup>3.</sup> The External Interrupt Address Vector is the Timer Address + H'0080' 5. F38T56 and F38T57 have F3871-type timer and strobe logic.

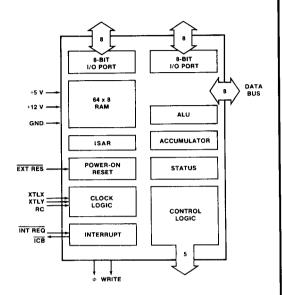
<sup>4.</sup> Three different types of timers and control ports exist. For further detail see Figures 1, 2, and 3.

## **F8 MICROPROCESSOR FAMILY**

# F3850 CENTRAL PROCESSING UNIT (CPU)

The CPU is an 8-bit arithmetic device with 70 instructions. It contains a 64-byte RAM, an instruction register, an accumulator, two parallel I/O ports, an interrupt control, power on reset and clock generation logic. The CPU provides communication control lines to the other members of the family.

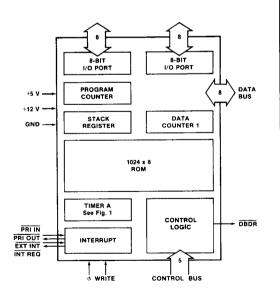
The F8 offers several alternatives for connecting memory to the system. These may be used individually, or in various combinations, depending upon the requirements.



F3850 CPU

#### F3851 PROGRAM STORAGE UNIT (PSU)

The F3851 PSU contains 1024 bytes of mask programmable ROM, a program counter and a data counter. It also has two parallel I/O ports, an 8-bit data port, a stack register, an incrementer/adder, a programmable timer and an interrupt control. Several F3851 circuits may be put in one system, thus increasing the ROM, I/O, and interrupt capability of the system. The F3851 program storage unit may be used alone, or in combination with one of the memory interface circuits.

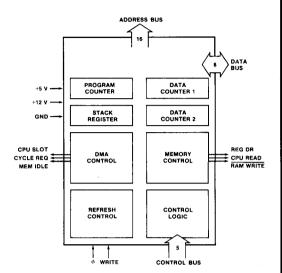


F3851 PSU

## **F8 MICROPROCESSOR FAMILY**

## F3852 DYNAMIC MEMORY INTERFACE (DMI)

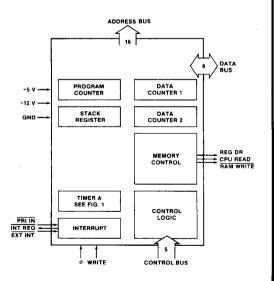
The DMI provides an appropriate interface for either static or dynamic memory components. When dynamic RAM circuits are used the DMI provides the necessary refresh controls required to maintain memory integrity. Another function of the DMI is to provide control for the F3854 DMA circuit. The dynamic memory refresh cycles and the DMA transfers are performed without slowing the central processor. The DMI also contains a program counter, data counter, an auxiliary data counter, stack register, incrementer/adder, an 8-bit data bus and a 16-bit address bus for communication with external memory. The DMI may be used solely with the CPU, or in conjunction with the F3851 PSU device.



#### F3852 DMI

# F3853 STATIC MEMORY INTERFACE (SMI)

The SMI is the second of three alternative devices in the F8 family which may be used with the 3850 CPU for memory interface. The SMI provides the necessary control for static memory components such as the 2102 RAM, 2708 EPROM, or 93448 PROM. The SMI also contains a program counter, data counter, an auxiliary data counter, stack register, incrementer/adder, a programmable timer, an 8-bit data bus and a 16-bit address bus for communication with external memory. The F3853 may be used solely with the CPU, or in conjunction with F8 PSU devices.



F3853 SMI

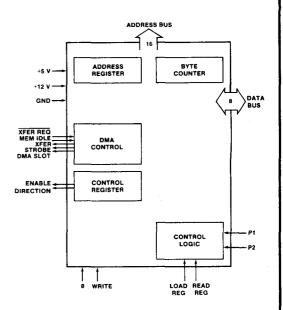
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## **F8 MICROPROCESSOR FAMILY**

# F3854 DIRECT MEMORY ACCESS UNIT (DMA)

The DMA circuit allows memory access from an external device during periods when the CPU is not using the memory. The F3852 DMI provides a control line which indicates periods when the memory is idle. During these periods the DMA transfers data between an external device and the memory. This operation is performed without slowing the central processor. In addition, the DMA contains a 16-bit memory address bus, an 8-bit data bus, programmable address vector and data length counter.



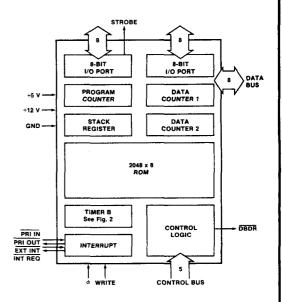
F3854 DMA

#### F3856 PROGRAM STORAGE UNIT (PSU)

It is important to note that Fairchild's program storage unit is not just a conventional read only memory. In addition to containing 2048 bytes of mask programmable ROM for program and constant storage, the F3856 includes the addressing logic for memory referencing, a program counter, an indirect address register (the data counter) and a stack register. A complete vectored interrupt level, including an external interrupt line to alert the central processor, is provided. All of the logic necessary to request, acknowledge and reset the interrupt is on the F3856. The 8-bit programmable timer is especially useful for generating real time delays. The PSU has an additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F3850 and two F3856 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 4096 bytes of ROM, 48 I/O bits, two interrupt levels, and two programmable timers. This complete system will require only three IC packages.

The F38T56 incorporates the F3871-type timer and strobe logic.



F3856 PSU

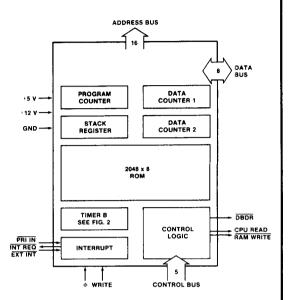
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## **F8 MICROPROCESSOR FAMILY**

## F3857 PROGRAM STORAGE UNIT/STAT-IC MEMORY INTERFACE (PSU/SMI)

The F3857 is the third alternative device in the F8 family which may be used with the F3850 CPU for memory interface. The PSU/SMI provides the necessary control for static memory components such as the 2102 RAM or F2708 EPROM. The PSU/SMI also contains a program counter, data counter, an auxiliary data counter, stack register, incrementer/adder, a programmable timer, an 8-bit data bus and a 16-bit address bus for communication with external memory. The F3857 may be used solely with the CPU, or in conjunction with other members of the F8 family. The F3857 differs from the F3853 in that a 2048 byte mask programmable ROM is also included.

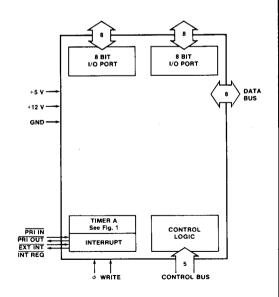
The F38T57 incorporates the F3871-type timer and strobe logic.



F3857 PSU/SMI

## F3861 PERIPHERAL I/O DEVICE (PIO)

The PIO is an expansion unit for I/O ports, interrupts and timers. It contains two 8-bit I/O ports, one interrupt control, and one programmable timer. Depending on the application requirements, multiple PIOs may be added to the system to expand the functions at low cost.

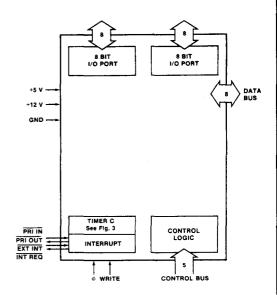


F3861 PIO

## **F8 MICROPROCESSOR FAMILY**

### F3871 PERIPHERAL I/O DEVICE (PIO)

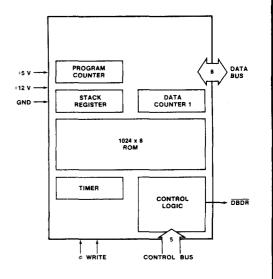
The PIO is an expansion unit for I/O ports, interrupts and timers. It contains two 8-bit I/O ports, one interrupt control, and one programmable timer. Depending on the application requirements, multiple PIOs may be added to the system to expand the functions at low cost. The versatile timer/interrupt circuit has the ability to measure external pulse widths, or count external pulses in addition to providing a timer with resolution of  $1.0 \mu s$  at 2.0 MHz.



F3871 PIO

### F3899 PROGRAM STORAGE UNIT (PSU)

The F3899 PSU contains 1024 bytes of mask programmable ROM, a program counter, stack register, and a data counter. The F3899 provides a low cost ROM memory to augment the F8 family.



F3899 PSU

## MICROMACHINE™ SERIES AND F8 FAMILY TIMERS

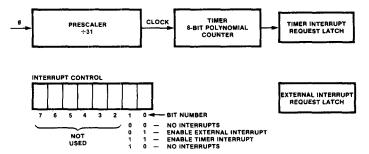


Fig. 1 Timer and Interrupt Control for F3851, F3853 and F3861

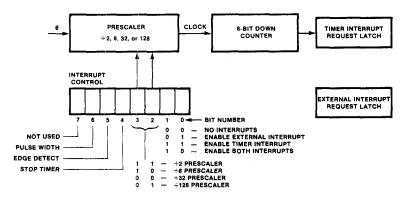


Fig. 2 Timer and Interrupt Control for F3856 and F3857

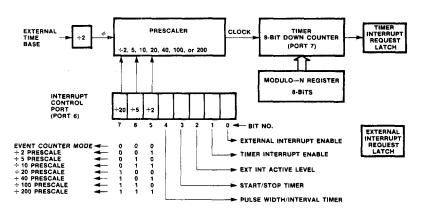


Fig. 3 Timer and Interrupt Control for F3870 and F3871



## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

The microprocessor system designer can now create his own hardware and software development systems by selecting modular subassemblies from Fairchild's Formulator design aids. He may start development with a Mark I singleboard system, then expand to more sophisticated Mark II or Mark IIFD development systems that can handle both software and hardware development. Or, he may graduate to a complete Formulator Mark III with intelligent front panel, power supply, and accessories or to the top of the line Formu-

lator Mark IIIFD with floppy disk drives.

Three growth packages plus a selection of optional modules provide a practical method for upgrading the single-board Mark I to either the Mark II or Mark IIFD or to the maximum system configuration Mark III or Mark IIIFD. Using the growth packages, the designer can begin sophisticated system application programs at very low cost and then upgrade his development tools in relatively inexpensive steps.

#### FORMULATOR MARK I

The first member of the Formulator family, the Formulator Mark I, is a basic microcomputer development tool providing the hardware necessary to build prototype systems. Included in the basic system is the Formulator Processor Module with the F8 CPU, Static Memory Interface, Dynamic Memory Interface, and Program Storage Unit devices. The Fairbug debug program, a 1K-byte monitor debug package, is included in the Program Storage Unit on the Processor Module. Fairbug provides the Mark I with sufficient debug capability to load a program, examine registers, monitor and alter memory locations, store a program on an external file. and generate a tape suitable for burning PROM memory devices. The Mark I also comes equipped with a 13slot card cage and motherboard for attaching the modular Formulator printed circuit boards. Cables and documentation are also included in the F8 Formulator Mark I system, including a peripheral interface cable which can connect the Mark I to a Teletype ASR33 or TI Silent 733 for external communication.

#### Hardware

Formulator Processor Module
Formulator Card Cage and Motherboard
Processor Module to Peripheral Cable
Power Cable
Cable Kit

#### Software

Fairbug Debug Program

#### Documentation

Formulator User's Guide Formulator Hardware Reference Manual Formulator Mark I Systems Coverage Manual Formulator Utilities Manual

#### FORMULATOR MARK II

The second member is the Formulator Mark II. This unit is a low cost microcomputer software and hardware development tool. It includes the basic hardware required to develop a system, as well as the necessary software tools to develop object code. The Mark II consists of all the components of the Mark I, namely the Processor Module, card cage and motherboard, cable kit, and the Fairbug debug program, as well as an additional 16K-byte RAM module. Also a part of the Mark II is the Formulator Operating System, including the editor, relocating assembler, and debug package to allow the generation of source code and to create and check out object code. Peripheral interfaces are also available to connect the Mark II to a TI Silent 733 or Teletype ASR33.

#### Hardware

Formulator Processor Module 16K-Byte RAM Module Formulator Card Cage and Motherboard Processor Module to Peripheral Cable Power Cable Cable Kit

#### Software

Formulator Operating System

#### Documentation

Formulator User's Guide Formulator Hardware Reference Manual Formulator Mark II Systems Coverage Manual Formulator Utilities Manual

## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

#### **FORMULATOR MARK IIFD**

The third member is the Formulator Mark IIFD, a floppy-disk based low-cost microcomputer software and hardware development tool. It includes the basic hardware required to develop a system, as well as the necessary software tools to develop programs. The Mark IIFD consists of all the components of the Mark I. namely the Processor Module, card cage and motherboard, cable kit, and the Fairbug debug program, as well as an additional 16K-byte RAM Module. The F8-DOS-III is also a part of the Mark IIFD. It includes a floppy-disk file manager, editor, relocating assembler. and debug package to generate source code and to create and check out object code. The Mark IIFD can communicate with teletype ASR33 and other standard RS232 CRT or printing terminals.

Hardware

Parallel Interface Module Prom Boot Loader Module Formulator Processor Module 16K-Byte RAM Module Formulator Card Cage and Motherboard Processor Module to Peripheral Cable Power Cable Cable Kit

#### Software

F8-DOS-III Floppy Disk Operating System

#### **Documentation**

Formulator User's Guide Formulator Hardware Reference Manual Formulator Mark II Systems Coverage Manual Formulator Utilities Manual

### FORMULATOR MARK III

The fourth level of microprocessor development equipment is the Formulator Mark III, offering all of the design assistance required to develop microprocessor systems. The combination of hardware, software, and firmware offered by the Mark III assists the designer from the generation of source programs through the development of a prototype system. The Mark III is a modular microcomputer that accommodates a variety of memory, input/output, and communication configurations to form a new and powerful development system. It contains all of the components of the Mark II—the Processor Module, card cage and motherboard, cable kit, the Fairbug debug program, 16K bytes of RAM, and the Formulator Operating System. In addition, the Mark III includes a Quad I/O Module with four I/O ports and two interrupts, a Communications Module with an onboard UART, a universal breadboard for building user hardware configurations, an extender module, and an intelligent operator's panel. Power supplies for the Mark III may be either 100 volts, 115 volts, or 220 volts at 50/60Hz. Peripheral interfaces are available to connect the Mark III with a TI Silent 733, a Teletype ASR33, or an HP 2645A Mini-Data Station.

#### Hardware

Formulator Mainframe Designer's Console with Firmware Formulator Processor Module 16K-Byte RAM Module Quad I/O Port Module Communications Module Universal Breadboard Extender Module Cable Kit User I/O Cable Assembly Communications Module to Peripheral Cable

#### Software

Fairbug Debug Program Formulator Operating System

#### **Documentation**

Formulator User's Guide Formulator Hardware Reference Manual Formulator Mark III Systems Coverage Manual Formulator Utilities Manual

#### FORMULATOR MARK IIIFD

equipment is the floppy-disk-based Formulator Mark IIIFD, offering all of the design assistance required to develop microprocessor based systems. The combination of hardware, software, and firmware offered by the Mark IIIFD assists the designer from the generation of source programs through the development of a prototype system. The Mark IIIFD is a modular microcomputer that accommodates a variety of memory, input/output, and communication configurations to form a new 100 volts, 115 volts or 220 volts at 50/60Hz. The Mark and powerful development system. It contains all of the IIIFD can communicate with teletype ASR33 or other components of the Mark IIFD, the Processor Module, standard RS232 glass or printing terminals.

The top of the line in microprocessor development card cage and motherboard, cable kit, the Fairbug debug program, parallel interface, PROM boot loader. 16K bytes of RAM, and the F8-DOS-III disk operating system. In addition, the Mark IIIFD includes a quad I/O module with four I/O ports and two interrupts, a communications module with an on-board UART, a universal breadboard for building user hardware configurations, an extender module, and an intelligent operator's panel. Power supplies for the Mark IIIFD may be either

## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

#### FORMULATOR MARK IIIFD (Cont'd)

#### Hardware

Cable Kit

Formulator Mainframe
Designer's Console with Firmware
Formulator Processor Module
Parallel Interface Module
PROM Boot Loader Module
16K-Byte RAM Module
Quad I/O Port Module
Communications Module
Universal Breadboard
Extender Module

User I/O Cable Assembly
Communications Module to Peripheral Cable

#### Software

F8-DOS-III Floppy Disk Operating System

#### **Documentation**

Formulator User's Guide Formulator Hardware Reference Manual Formulator Mark III Systems Coverage Formulator Utilities Manual

#### **F8-DOS-III DESCRIPTION**

The Formulator F8-DOS-III operating system provides floppy-disk bulk storage capability for Fairchild's Formulator Mark IIFD and Mark IIIFD F8 microcomputers when used with up to four plug-compatible iCOM® series FD 360, FD3700 and Frugal Floppies™ providing for over one megabyte of total storage capacity.

F8-DOS-III provides a powerful and complete development software package with batch operation, linking loader, and relocating assembler, and provides an easy to use, reliable, fast and extremely efficient capability for auxiliary program and data storage during F8 and F3870 software development or in end-user applications.

iCOM® Advertised	F8-DOS-III SUMMARY						
FD3700 Series Features	Disk Monitor	Editor	Relocating Assembler	Real-Time Debugger			
Fully IBM 3740 media and	Assemble	Move Line	No-List Option	Symbolic Debugging			
format compatible	(Relocating)	Copy Line	No-Object Option	Set Up to 8 Breakpoin			
Full formatter and controller	Load (Linking)	Bottom	Error Messages	Clear Breakpoint			
built-in	List Directory	Change	Invalid Label	Clear All Breakpoints			
Full sector Read/Write buffers	Print File	Delete	Duplicate Label	Continue Execution			
allow asynchronous or DMA	Rename File	File	Invalid Op Code	Go To Location			
data transfer	Create File	Find String	Operand Error	Return to Monitor			
Drive and diskette Write Pro-	Delete File	Insert	Syntax Error	Single Step			
tect capability	Copy File	Locate String	Undefined Symbol	Trace On Long			
Positive latching door	Copy Disk	Next	Expression Storage	Trace On Short			
mechanism	GenMod	Replace	Overflow	Trace Off			
Up to 4 drives with no soft-	(Created	Tab	Relocatability	Display Memory			
ware or hardware modifi-	Linked File)	Тор	Error	Display Register			
cations	Edit Mode						
MTBF in excess of 2300 hours		Type	Pseudo Operand	Display Port			
(FD 3712 dual drive)	Load (Absolute)	Up .	Error	Store Memory			
Plug-in convenience allows	DeBug Mode		Cross Reference	Store Register			
MTTR of 18 minutes	Assign Virtual I/O			Store Port			
Front panel LED status	Burn PROM		,				
indicators	Convert						
LED drive select indicators	ROM Dump						
Fully retracting head and							
pressure pad for maximum							
diskette life							
50 pin flat ribbon cable with							
3M interface connector—							
FD 360 compatible							

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## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

#### FORMULATOR GROWTH PACKAGES

The Mark I, Mark II, and Mark III Formulator systems previously described are all upwards compatible. The Mark I can be expanded to become a Mark II; likewise, the Mark II may be developed into a Mark III. In addition, a Mark II can be expanded to a Mark IIFD and a Mark III into a Mark IIIFD. This means that a microprocessor system designer may enter the microcomputer design at a level which best matches the needs at handamount of available money, time, microprocessor experience—and be able to increase the Formulator's capabilities as his needs grow. Three growth packages are available to Formulator product owners. Growth Package 1 converts a Mark I system to a Mark II: Growth Package 2 extends the capabilities of the Mark II into the Formulator Mark III, and Growth Package 3 extends a Mark II or III into a Mark IIED or IIIED.

#### Growth Package I

16K-Byte RAM Module
Mark II Formulator Operating System

#### Growth Package 2

Quad I/O Module
Communications Module
Power Supply
Fan
Console Control Modules
Internal Cable Wiring
Universal Breadboard
Extender Module
I/O Cable Assembly
Communications Module to Peripheral Cable
Mark III Formulator Operating System

#### **Growth Package 3**

Parallel Interface Module PROM Boot Loader Module F8-DOS-III System Diskette

#### PERIPHERAL OPTIONS

The Formulator Mark II systems interface with either a Teletype ASR33 with the auto read/auto punch option or a TI Silent 733 ASR with the ADC option. The teletype terminal provides a paper tape based system, while the 733 allows file storage on magnetic tape cassettes. To decrease load times, a Remex high speed paper-tape reader (or equivalent) may be used with either peripheral unit.

The Formulator Mark III provides an interface for the HP Mini-Data Station as well. This high speed unit combines the efficiency of the magnetic tape cartridges with an intelligent terminal and thermal line printer to allow the rapid development and debugging of application programs.

The Formulator Mark IIFD and IIIFD systems interface with any standard RS232 terminal and printer or printing terminal to offer maximum peripheral cost/speed flexibility.

#### **HP MINI-DATA STATION**

The HP 2645A Mini-Data Station features an interactive CRT Terminal with high resolution display and a fully integrated mass storage capability, making it easy to use both on- and off-line. It uses 2-1/2" x 3-1/4" x 1/2" magnetic cartridges which store up to 110 kilobytes of formatted data. The Mini-Data Station has two mini

cartridge drives, allowing for a total of 220 kilobytes of data storage on magnetic tape. Thus, all files—both operating system and user files—are resident on the magnetic tape. Loading and storing files is accomplished by reading and writing onto the cartridge. The user's time is decreased and efficiency increased when the magnetic tapes are used.

The 2645 Mini-Data Station comes equipped with three data cartridges, an Owner's Manual, and an Installation and Service Manual.

#### **HP 9866A PRINTER SUBSTATION**

The HP 9866A line printer is a moderately priced, high performance companion to the HP 2645A Mini-Data Station, providing a permanent record of the contents of the Mini-Data Station display and memory for future use. The printer operates at up to 240 lines per minute with a maximum line width of 80 characters. The character set consists of 64 alphanumeric characters generated by a 5 x 7 dot matrix. Since a thermal printing mechanism is used to make this printer quiet enough for normal office use, thermal sensitive paper is required. This paper is 8-3/4 inches wide and available in 250 foot rolls.

The 9866A thermal printer comes equipped with two rolls of paper, a power cord, an interface card and cable, and an Instruction Manual.



## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

#### **ICOM F3712 DUAL FLOPPY DISK**

The iCOM FD3700 Series Floppy Disk System for microcomputers continues the tradition of the iCOM FD360. The FD3700 brings to the OEM, and to the development lab, proven reliability and popular features, while incorporating advanced styling and new convenience items.

#### The iCOM FD3700 Series features the following:

- Fully IBM 3740 media and format compatible
- · Full formatter and controller built in
- Full sector read/write buffers allow asynchronous or DMA data transfer
- Drive and diskette write-protect capability
- · Positive latching door mechanism
- Up to four drives with no software or hardware modifications
- MTBF in excess of 2300 hours (FD3712 dual drive)
- Plug-in convenience allows MTTR of 18 minutes

- · Front panel LED status indicators
- · LED drive select indicators
- Fully retracting head and pressure pad for maximum diskette life
- 50-pin flat ribbon cable with 3M interface connector—FD360 compatible

#### iCOM Performance features are as follows:

- Disk speed 360 RPM ± 1.5%
- 10 ms track-to-track access time
- 40 ms head load time
- · 5 ms sector read/write time
- 83 ms average latency time
- 700 ms automatic head unload time
- 1 ms interrecord time

#### **Power Requirements Are:**

110-125  $V_{ac}$ , 60Hz, 200 W max Optional 220-240  $V_{ac}$ , 50Hz, 200 W is available

#### **OPTIONAL FORMULATOR MODULES**

Expansion of the Formulator microcomputers need not occur along the path indicated by the growth packages. Optional Formulator modules are available to expand RAM, PROM I/O, and communications, so the user can develop a custom system which is perfectly suited to his specific needs. These optional modules may be attached to the Formulator via the 13 card slots in the motherboard. The first three slots are dedicated to front panel operations of the Mark III. Another slot is reserved for the Processor Module. The remaining nine slots are linked on a common bus whose signals are compatible with the modules themselves. Additional system functions may be easily added to any Formulator system by simply plugging in one of the modules. Thus, the initial Formulator investment is preserved.

Nothing needs to be discarded as demands upon the system increase. Unless otherwise noted, all of the following optional modules are available to update any Mark I, Mark II, Mark IIFD, Mark III, or Mark IIIFD system to meet expanded requirements.

#### **Optional Modules**

4K-Byte RAM Module
16K-Byte RAM Module
Quad I/O Port Module
4K-Byte PROM Module
Communications Module
Byte Parallel Interface Module
ROM Simulation Module
Universal breadboard
Extender Module
I/O Light Display Board

#### **PROM PROGRAMMER**

The ability to easily program permanent memory devices is essential to any microprocessor design. The Formulator PROM Programmer connects to a Quad I/O Module within either a Formulator Mark II or a Formulator Mark III, permitting the programming of any of the following fuseable link or ultraviolet light eraseable PROMs from a pattern stored in the Formulator memory.

The 11" x 12" x 4" PROM Programmer is driven by a utility program contained within the Formulator Operating System and features a simple, easy to use com-

mand set. The commands, entered into the PROM Programmer from the Formulator peripheral via the keyboard, allow the user to transfer data from a PROM to memory, burn a PROM, verify a PROM pattern, manually enter a single byte of data, and display PROM locations using the system software. The programming idiosyncrasies of each PROM are contained in software look-up tables to relieve the user of intricate repetitious set-up. The procedure is simply to identify the PROM type (like 93448) and the PROM parameter look-up table is automatically invoked, defining such things as number of words, word bit length, burn time, wait time, retry conditions, etc. The programming is convenient

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## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

#### PROM PROGRAMMER (Cont'd)

enough to allow the PROM Programmer to be used in a production environment.

Included in the basic system are two socket boards, one for the Fairchild 93436/93446 PROMs and one for the 93438/93448 PROMs. Socket boards for the ultraviolet eraseable devices are also available. A cable to the Quad I/O Module and a power cord are also included in the basic unit.

Fairchil	d Fu	sible
Link F	PRO	MS

Ultraviolet Eraseable PROMs

93436	(512	x 4	)
93446	(512	x 4	)
93438	(512	x 8	)
93448	(512	x 8	)

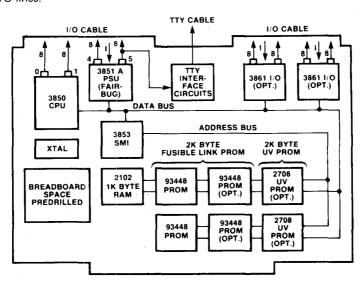
2704 (512 x 8) 2708 (1024 x 8)

### OCM-1 ONE-CARD MICROCOMPUTER

The OCM-1 is a complete microcomputer system contained on a single printed circuit board and offering the following features:

- 64-byte scratch pad memory
- 1K-byte RAM
- 8K-byte ROM (1K supplied, sockets provided for balance)
- 4K-byte EPROM (sockets provided)
- 4K-byte PROM (sockets provided)
- Up to four programmable timers
- Up to four programmable interrupts
- RS232 interface (current loop optional)
- 2MHz clock
- Self-contained Fairbug teletype operating system
- Up to 64 individually programmable, bidirectional, latched I/O lines.

The unit is based on the F8 microcomputer and is fully supported by the Formulator family of program development aids. In addition, the OCM-1 contains a built-in teletype operating system, called Fairbug I, contained in the F3851A Program Storage Unit. Using an OCM-1to-TTY cable assembly, the board can be directly coupled to a teletype or RS232 terminal to display or alter memory location, to load and punch paper tape, or to make entries from the keyboard or by program instruction. An alternative built-in operating system, K-D Bug, contained in the F3856A PSU is also available. It provides all of the Fairbug I functions plus a resident monitor to facilitate operation with a low-cost calculator-style keyboard and LED display. A Fairbug user's guide is provided with the OCM-1. The K-D Bug should be ordered as a separate item.



## MICROMACHINE™ SERIES AND F8 FAMILY DESIGN AIDS

### ONE CARD MICROCOMPUTER (Cont'd)

The OCM-1 processor section includes the 3850 Central Processing Unit, the F3853 Static Memory Interface, a 2MHz clock, and reset circuitry.

The OCM-1 memory section contains the capability for the use of five different types of storage including 64 bytes of scratch pad, 1K bytes of RAM, sockets for 2K bytes of EROM (2708), sockets for 2K bytes of fusible link PROM (93448), and the Fairbug I operating system.

The I/O portion of the system is contained in the F3850 Central Processing Unit and a F3851A Program Storage Unit, each containing two 8-bit I/O ports. Two sockets are provided for inserting standard F8 PIO circuits (F3861 or F3871) or, if more ROM is required, standard PSUs (F3851 or F3856) may be inserted. In either case, four additional I/O ports are provided bringing the maximum total to eight I/O ports (64 lines). Only single-byte instructions are required to individually program these lines for either input or output functions. Latches on each line reduce external hardware cost. A circuit on the board gives the OCM-1 the capability of communicating with a teletype, RS232 device or 20mA current loop.

In its standard configuration, the OCM-1 contains two interrupts and two timers, one in the F3851A PSU and one in the F3853 SMI. Two additional interrupts and timers may be added by plugging the two additional PIOs into their sockets. A "daisy-chained" priority system determines which interrupt will be serviced if two or more requests are made simultaneously.

The OCM-1 requires three power supply voltages:  $\pm 12V$  @ 0.255 A,  $\pm 5V$  @ 0.4 A and  $\pm 5V$  @ 0.09 A. The  $\pm 5V$  supply is used only for the 2708 EROM devices. All supply voltages are  $\pm 5V$  maximum.

The entire microcomputer is contained on a single board (epoxy glass with solder mask) measuring approximately 7.5 inches by 10.5 inches. It includes a 2-inch by 4-inch pre-drilled breadboarding area for users who want to develop unique system configurations. In addition, a Formulator-compatible 100-pin edge connector, a special connector for TTY or terminal, and two 44-pin edge connectors for F8 signals, are contained on the board. A switch to enable the Fairbug operating system is also provided. The OCM-1 is delivered completed with OCM-1 Users Manual, Fairbug Users Guide and F8 Guide to Programming.

#### FORMULATOR SUPPORT

In addition to the optional boards, peripherals, cables, and other accessories, the Mark I, Mark II, and Mark III Formulator systems are supported by a wide range of documentation, and an intensive training program.

#### FORMULATOR DOCUMENTATION

The Formulator user has access to a full range of reference and instructional manuals to aid him in his system design and programming.

#### F8 USER'S GUIDE

The F8 User's Guide is a detailed description of the F8 family of microprocessor devices. Microprocessor systems are discussed, with the configurations of the F8 circuits examined in depth. The User's Guide also outlines the F8 instruction set. Detailed specifications of each member of the F8 microprocessor family is given, including functional descriptions, logic diagrams, signal load levels, and timing diagrams for each circuit. Typical F8 system configurations are also presented.

#### MICROMACHINE USER'S GUIDE

The Micromachine 2 User's Guide is a detailed description of the F3870, F38770, F3872 and F3874 Micromachines. This manual covers programming and systems design with emphasis on application implementation.

#### **GUIDE TO PROGRAMMING**

The Guide to Programming is written for logic designers with little or no background in computer programming. It introduces machine and assembly language programming to the potential user of microprocessors and microcomputer systems. Introductory topics include flowcharting, memory allocation, source and object programs, and assembly language. More advanced topics include programmed I/O, interrupts, programmable timers, subroutines, macros, data manipulation, and programmed direct memory access channels. Numerous examples of these programming techniques are given.

#### **FORMULATOR USER'S GUIDE**

The Formulator User's Guide fully describes the operation of the Formulator Development system. It covers the Mark I, Mark II, and Mark III hardware configurations and contains a detailed description of the Formulator software—the monitor, the editor, the assembler, and the debug program. The F8 DOS-III User's Guide is also available for Mark IIFD and Mark IIIFD systems.

#### FORMULATOR HARDWARE REFERENCE MANUAL

This book presents an in-depth technical description of the F8 Formulator System, its component subsystems, and options. The technical description includes general functional characteristics, theory of operation, and detailed description of interface signals.

#### **FAIRCHILD LOGIC/CONNECTION DIAGRAMS**

